Refine Search

Search Results -

Terms	Documents
L4 and dma	1

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Saturday, March 31, 2007 **Purge Queries** Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L6	l4 and dma	1	L6
L5	L4 and repeated$	0	L5
L4	5448728[pn]	1	L4
L3	L2 same dma	30	L3
L2	writable-once or wo or (write adj1 once)	410148	L2
L1	7188271[pn]	1	L1

END OF SEARCH HISTORY

L3: Entry 26 of 30 File: USPT Sep 5, 1995

DOCUMENT-IDENTIFIER: US 5448728 A
TITLE: Storage medium control system for controlling a write-once read-many storage medium

Brief Summary Text (12):
According to a third aspect of the invention, a system for accessing a write-once read-many storage medium is arranged so that the writing mechanism serves to read the data written on the data storage area by using DMA (direct memory access) transfer in order to search the non-writing area.

Drawing Description Text (9):
FIG. 8 is an explanatory view showing a DMA transfer executed in a system for accessing a write-once read-many storage medium according to a third embodiment of the invention:

Detailed Description Text (21):
In turn, the description will be directed to a system for accessing a write-once read-many storage medium according to a third embodiment of the present invention as referring to FIGS. 8 and 9, in which FIG. 8 is an explanatory view showing a DMA (Direct Memory Access) transfer executed in this embodiment and FIG. 9 is a flowchart showing the operation of this system. In the second embodiment, the accessing system is arranged to read all the stored data on the written area F1 into the memory and search the head address of the non-writing area F2. This arrangement results in consuming a long processing time of the CPU 11 such as a ready-check time and a seek time. On the other hand, in this embodiment, the accessing system further includes a DMA controller for reducing the processing time of 3 u the CPU 11.